REPLY UNDER 37 C.F.R. 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2124
PATENT
Application # 09/697,419
Attorney Docket # 1999P07938US01 (1009-045)

REMARKS

The Examiner is respectfully thanked for the thoughtful consideration provided to this application. Reconsideration of this application is respectfully requested in light of the following remarks.

Claims 4 – 11 are now pending in this application. Each of claims 4, 5, 7, 9, and 11 are in independent form.

I. The Obviousness Rejections

Each of claims 4-11 was rejected under 35 U.S.C. 103(a) as being unpatentable over various combinations of Moran (U.S. Patent No. 5,519,843) in view of Stripf (U.S. Patent No. 6,263,487). These rejections are respectfully traversed.

Applicant filed a 37 CFR § 1.132 Declaration of Dr. Ronald D. Williams, a professor of engineering at University of Virginia, and one skilled in the art of electrical engineering with a Reply to a prior Office Action (the Reply dated 2 May 2005). On 19 August 2005, Applicant filed a replacement copy of that Declaration, signed 18 August 2005, to correct a typographical error noted by the Examiner in the present Office Action.

None of the applied references, either alone or in any combination, establish a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable

expectation of success must both be found in the prior art, and not based on applicant's disclosure." *See* MPEP 2143.

A. Moran Uses Three Chips

Each of independent claims 4, 5, 7, 9, and 11 recite, yet Moran fails to expressly or inherently teach or recite, "**a single chip** program execution device" "**lacking a memory device external to said single chip** program execution device."

Paragraphs 11-18 of Dr. Williams' Declaration provided evidence that one skilled in the art would not find that Moran expressly or inherently teaches or recites "**a single chip** program execution device" "**lacking a memory device external to said single chip** program execution device." Stripf does not overcome the deficiencies of Moran.

The present Office Action recites "Applicant has submitted that Moran uses 3 chips (Appl. Rmrks, pg. 7, bottom) without further evidence supporting this allegation with respect to the cited portions of Moran. It is noted that the rejection has cited a single integrated chip (ASIC). Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." *See* Page 12.

With all due respect, this statement from the present Office Action is baseless and without merit.

Under 37 CFR 1.111(b) a "reply must present arguments pointing out the specific distinctions believed to render the claims, including any newly presented claims, patentable over any applied references." Applicant respectfully submits that the Reply dated 2 May 2005 fully complies with 37 CFR 1.111(b) in all respects.

To reiterate, each of independent claims 4, 5, 7, 9, and 11 recite, yet Moran fails to expressly or inherently teach or recite, "**a single chip** program execution device" "**lacking a memory device external to said single chip** program execution device."

Dr. Williams' Declaration provides persuasive evidence that Moran uses **three chips**. Moran allegedly recites, as evidence regarding three chips, that "FIG. 2 is a block diagram of an exemplary **system** according to the present invention." See col. 2, lines 39-40. In describing FIG. 2, Moran allegedly recites "FIG. 1 very generally illustrates a layout of some of the **typical components of such systems**, including **a CPU or microprocessor 10, a system memory (RAM) 12**, a ROM BIOS chip 14, and a hard disk drive unit 16, **all of which receive data from**, and place data on, **a system bus 18**. According to exemplary embodiments of the present invention, **the ROM BIOS chip is replaced by a flash memory system chip which includes the BIOS as well as a solid state disk** which is designed to emulate, for example, storage provided by a hard disk unit. Such a system is shown by the block diagram of FIG. 2, wherein the flash memory system 20 replaces the ROM BIOS chip 14." See col. 2, line 63 – col. 3, line 8. Moran's "flash memory system chip" does not expressly or inherently teach or suggest a "program execution device". Rather, Moran's "program execution device is "CPU or microprocessor 10". Thus, Moran's "system" comprises "**a CPU or microprocessor 10,**" "**a system memory (RAM) 12,**" and a "**flash memory system chip**" coupled via a "**system bus 18.**" *See* FIG. 2.

Applicant respectfully requests an explanation as to how Moran's system comprising three separate chips, including two memory chips external to the "program execution device" coupled by a bus can possibly expressly or inherently teach or recite "**a single chip** program execution device" "**lacking a memory device external to said single chip** program execution device" as claimed in each of independent claims 4, 5, 7, 9, and 11.

In further response to Applicant's prior Office Action Reply dated 2 May 2005, the present Office Action recites "[t]his is not an anticipation type of rejection per se; and in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references." *See* Page 13.

With all due respect, Applicant respectfully points out that neither Moran nor Stripf expressly or inherently teaches "**a single chip** program execution device" "**lacking a memory device external to said single chip** program execution device" as claimed in each of independent claims 4, 5, 7, 9, and 11. Accordingly Applicant respectfully requests an explanation of how two references missing a claimed element can be combined to teach or recite that missing element.

Thus, even if there were motivation or suggestion to modify or combine the applied references (an assumption with which the applicant disagrees), and even if there were a reasonable expectation of success in combining or modify the applied references (another assumption with which the applicant disagrees), the combined applied references still do not expressly or inherently teach or suggest **every** limitation of the independent claims, and consequently fail to establish a *prima facie* case of obviousness.

Because no *prima facie* rejection of any independent claim has been presented, no *prima facie* rejection of any dependent claim can be properly asserted. Consequently, reconsideration and withdrawal of these rejections is respectfully requested.

B. Unsupported Official Notice

In Applicant's Reply, dated 2 May 2005, to the prior Office Action, Applicant respectfully traversed the Official Notice is taken to support the rejections. Applicants requested citation and provision of references supporting the rejections. *See* MPEP 2144.03.

In that Reply, Applicant pointed out that:

> [s]pecifically, each of independent claims 4, 5, 7, 9, and 11 recite a "**programmable logic controller.**" The present Office Action recites "Moran discloses a **programmable controller** (Fig. 9)." See Page 3. The present Office Action [the Office Action dated 4 January 2005] further recites "an integrated controller (see Fig. 9) and the use of code to emulate more than one type of devices (see col.7, lines 14-23) wherein a programmable memory stores user programs for effecting logic to implement the control over an OS and related functionalities as taught by Moran (see SUMMARY) suggests a form of programmable logic controller, and the concept of emulation/simulation of multiple devices requiring control is suggested." See Page 4. Paragraphs 19-26 of Dr. Williams' Declaration provide evidence that one skilled in the art would not find that Moran expressly or inherently teaches or recites a "programmable logic controller."

In response to this, the present Office Action recites essentially the same arguments for rejection and in reply to Applicants argument by reciting "Moran is not explicitly teaching a actual PLC; but provides a integrated controller in a single chip (see Fig. 3,6), thus has shown sufficient teaching that such chip is a controller. The intended use of such integrated controller can include manipulating of data with complex operations or control of industrial switching of devices, but that is not the intended use that made Moran's become a patent, nor does it impart any patentable weight even if claimed in this instant application." See Page 13.

Applicant respectfully submits that even if this statement were not erroneous, a premise which applicant respectfully traverses, it fails to comply with the requirements of MPEP 2144.03. Applicant respectfully requested a reference supporting the apparent Official Notice taken in both the Office Action dated 4 January 2005. The present Office Action fails to provide

such a reference. Applicant reiterates the request for a reference supporting this unsupported Official Notice reiterated by the present Office Action.

Accordingly, Applicant respectfully requests the withdrawal of the finality of the present Office Action. Applicant further requests the withdrawal of each of the rejections of claims 4, 5, 7, 9, and 11 based upon this apparent Official Notice.

C. Unsupported Inherency Argument

In Applicant's Reply, dated 2 May 2005, to the prior Office Action, Applicant pointed out that:

> Moran fails to properly establish inherent anticipation of claim elements claimed in the present Office Action. *See* MPEP 2112. "Inherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." Trintec Indus., Inc. v. Top-U.S.A. Corp., 295 F.3d 1292, 1295, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002). No evidence has been presented that the admittedly "missing descriptive material is 'necessarily present'" in Moran. For example, the present Office Action recites [the Office Action dated 4 January 2005]:
>
> 1. "[n]or does Moran explicitly teach that the programmable controller is being implemented for executing a compilation is to implement PLC I/O functions and that the compilation comprises system support kernel. But in view of Moran's teachings as to be able to initialize the power settings or memory input/output resetting of the controller (e.g. col.3, lines 16 to col. 5, line 35; Fig. 7), such kernel related support instructions as well as input/output routines or I/O functions are strongly **implied** if not disclosed. See Page 4; and
> 2. "[n]or does Moran explicitly specify a single chip program execution device separable for a communication/programming device; but in view of the teachings of

user code being flashed into a single device for emulating a hard drive of the device (see Fig. 9; col. 6, line 59 to col. 7, line 3), this limitation is disclosed." See Page 5;

3. "[n]or does Moran explicitly disclose compiling to form said binary programmable logic control program; however, Moran teach no source code for being loaded in memory for execution, only user program being loaded to support the BIOS system functionality of the controller (col. 7, line 59 to col. 7, line 3). Hence this compiling limitation is **implicitly** disclosed." See pages 6-7.

Applicant respectfully requested evidence demonstrating that the admitted "missing descriptive material is 'necessarily present'" in Moran. While the present Office Action discusses each of these premises, absolutely no evidence is provided that indicates that the admittedly "missing descriptive material is 'necessarily present'" in Moran.

Accordingly, Applicant respectfully requests the withdrawal of the finality of the present Office Action. Applicant also respectfully request withdrawal of the rejections based thereon.

D. Moran Does Not Teach or Suggest Programmable Logic Controller I/O Functions

Independent claim 4 recites "programmable logic controller I/O functions." Paragraphs 27-32 of Dr. Williams' Declaration provides evidence that one skilled in the art would not find that Moran expressly or inherently teaches or recites "programmable logic controller I/O functions." Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 4.

In response to this argument, the present Office Action recites that the "USC 103 rejection does not address a I/O functions features but mainly focuses on rendering the making of a controller into a PLC an obvious limitations. There is no remote allusion to an expressed or inherent teaching by Moran concerning a PLC from the rationale as set forth in the rejection

because this rejection is a combination of teachings according to prima facie, and not one single reference is to be attacked individually." See Page 15.

To the extent that Applicant understands this argument, Applicant respectfully points out that a *prima facie* case of obviousness cannot be made unless all claimed elements are found in the applied references. A "USC 103 rejection" that "does not address a I/O functions features but mainly focuses on rendering the making of a controller into a PLC an obvious limitations" does not result in a *prima facie* case of obviousness with respect to claim 4 since all elements recited in the claim are admittedly not present in the applied references.

Accordingly, Applicant respectfully requests withdrawal of the rejection of claim 4.

E. Placing a Single Chip Program Execution Device in Stripf Would Render Stripf Inoperative

It is inappropriate to combine references when the combination "would produce a seemingly inoperative device." See, Nat's Steel Car, Ltd. v. Canadian Pac. Ry., Ltd., 357 F.3d 1319, 1339 (Fed. Cir. 2004); Tec Air Inc. v. Denso Mfg. Mich. Inc., 192 F.3d 1353, 1360 (Fed. Cir. 1999) (quoting In re Sponnoble, 405 F.2d 578, 587 (CCPA 1969).

Paragraphs 33-38 of Dr. Williams' Declaration provided evidence that one skilled in the art would find combining elements alleged to be present in Moran with Stripf would render at least Stripf inoperative for its intended purpose.

Thus, even if Moran disclosed claim limitations asserted in the present Office Action, a premise that Applicant disputes, attempting to combine Moran with Stripf would cause Stripf's programmable logic controller to cease functioning according to the "**requirements**" disclosed therein. Thus, one skilled in the art would find no motivation or suggestion to modify or combine the applied references. With or without Stripf, Moran fails to establish a *prima facie* obviousness rejection.

This traverse of the combination of Moran with Stripf stands. While the present Office Action discusses the persuasive evidence in Dr. Williams' Declaration, it concludes that "the affidavit remarks do not appear to build their ground based on the claimed language. There is no convincing evidence from the claim or from Moran that would render the integrated chip unfit to be used as a PLC; and there no teaching anywhere in the claim that enforces a PLC code being necessarily dynamically relinked as opposed to a code flashed into a chip; and there is no teaching anywhere in Moran or in Stripf that dictates that once a program is flashed, a flash program cannot be utilized in a PLC (**)." See Page 16.

To the extent that Applicant understands this response, Applicant reiterates the relevant legal standard regarding combining references:

> it is inappropriate to combine references when the combination produces a "seemingly **inoperative device**". See, Nat's Steel Car, Ltd. v. Canadian Pac. Ry., Ltd., 357 F.3d 1319, 1339 (Fed. Cir. 2004); Tec Air Inc. v. Denso Mfg. Mich. Inc., 192 F.3d 1353, 1360 (Fed. Cir. 1999) (quoting In re Sponnoble, 405 F.2d 578, 587 (CCPA 1969).

Applicant's evidence demonstrates that combining Moran with Stripf would produce an "**inoperative device.**" Accordingly, the present Office Action fails to present a *prima facie* case of obviousness for any of independent claims 4, 5, 7, 9, and 11.

Because no *prima facie* rejection of any independent claim has been presented, no *prima facie* rejection of any dependent claim can be properly asserted. Consequently, reconsideration and withdrawal of these rejections is respectfully requested.

F. Declaration Under 37 CFR 1.132

The present Office Action recites the "declaration under 37 CFR 1.132 filed 5/2/2005 is insufficient to overcome the rejections of claims 4-11 based upon a rejection using Moran under

35 USC §103 as set forth in the last Office action because it refer(s) only to the system described in the above referenced application and not to the individual claims of the application. Thus, there is no showing that the objective evidence of nonobviousness is commensurate in scope with the claims."

Applicant respectfully traverses this assertion.

Paragraphs 11 and 18 of Dr. Williams' initial and replacement Declarations specifically contrast the claim language of each of independent claims 4, 5, 7, 9, and 11 to the alleged teachings of Moran.

Further, paragraphs 19 and 26 of Dr. Williams' Declarations specifically contrast the claim language of each of claims 4-11 to the alleged teachings of Moran.

In addition, paragraphs 20 and 32 of Dr. Williams' Declarations specifically contrast the claim language of claim 4 to the alleged teachings of Moran.

Thus, Applicant respectfully submits that the assertion that the "declaration under 37 CFR 1.132 filed 5/2/2005 is insufficient to overcome the rejections of claims 4-11" is without basis.

Accordingly, Applicant respectfully requests the withdrawal of each rejection of claims 4-11.

II. Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

> "none of the references of record alone or in combination disclose or suggest the combination of limitations found in the independent claims. Namely,
>
> - claim 4 is allowable because none of the references of record alone or in combination disclose or suggest 'a single chip program execution device' 'a single chip program execution device comprising: a micro controller operable to

implement programmable logic controller I/O functions upon executing a compilation comprising the user program and a system support kernel, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program; and a re-programmable read only memory within which the compilation is stored, said single chip program execution device separable from a communication/programming device adapted to convert the user program to a binary code module and combine the binary code module with the system support kernel into a single executable firmware module, said programmable logic controller lacking a memory device external to said single chip program execution device';

- claims 5 and 6 are allowable because none of the references of record alone or in combination disclose or suggest 'receiving a symbolic user program at a communication/programming device, said communication/programming device separable from a single chip program execution device having a re-programmable read only memory, said single chip program execution device adapted to execute a binary programmable logic control program, said binary programmable logic control program stored within said re-programmable memory, said binary programmable logic control program adapted to operate a programmable logic controller, said programmable logic controller lacking a memory device external to said single chip program execution device; and compiling, at said communication/programming device, said symbolic user program to a binary code module; and combining the binary code module with a system support kernel to form said binary programmable logic control

program, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program';

- claims 7 and 8 are allowable because none of the references of record alone or in combination disclose or suggest 'receiving, from a communication/programming device, a binary programmable logic control program at a single chip program execution device having a re-programmable read only memory, said communication/programming device separable from said single chip program execution device, said binary programmable logic control program comprising a compilation of a symbolic user program combined with a system support kernel to form a single executable module, the system support kernel adapted to provide a programmable logic controller with operating system functions comprising sequencing the user program, said single chip program execution device adapted to execute said binary programmable logic control program to operate a programmable logic controller, said programmable logic controller lacking a memory device external to said single chip program execution device; and loading said binary programmable logic control program into said re-programmable read only memory of said program single chip execution device';

- claims 9 and 10 are allowable because none of the references of record alone or in combination disclose or suggest 'within a single chip, a program execution device having a re-programmable memory, said program execution device adapted to execute a binary programmable logic control program, said binary

programmable logic control program stored within said re-programmable memory, said binary programmable logic control program comprising a compilation of a user program and a system support kernel, said binary programmable logic control program adapted to operate a programmable logic controller, said programmable logic controller lacking a memory device external to said single chip program execution device; and a communication/programming device separable from said program execution device, said communication/programming device providing functions required for external communication of said binary programmable logic control program, said binary programmable logic control program comprising a binary module formed from compiling a symbolic user program, the binary module combined with a system support kernel to form a single executable module, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program, said communication/programming device adapted to load said binary programmable logic control program into said re-programmable memory and wherein said binary programmable logic control program is stored in said re-programmable memory of said program execution device by direct manipulation of logic controls of said re-programmable memory'; and

- claim 11 is allowable because none of the references of record alone or in combination disclose or suggest 'receiving a symbolic user program at a communication/programming device, said communication/programming device separable from a single chip program execution device having a re-programmable read only memory, said single chip program execution device

adapted to execute a binary programmable logic control program, said binary programmable logic control program stored within said re-programmable memory, said binary programmable logic control program adapted to operate a programmable logic controller, said binary programmable logic control program comprising a binary module derived via compiling a symbolic user program, the binary module combined with a system support kernel to form a single executable module, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program, said programmable logic controller lacking a memory device external to said single chip program execution device; and compiling, at said communication/programming device, said symbolic user program with a system support kernel to form said binary programmable logic control program".

REPLY UNDER 37 C.F.R. 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2124
PATENT
Application # 09/697,419
Attorney Docket # 1999P07938US01 (1009-045)

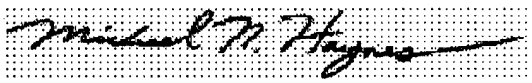
CONCLUSION

It is respectfully submitted that, in view of the foregoing amendments and remarks, the application as amended is in clear condition for allowance. Reconsideration, withdrawal of all grounds of rejection, and issuance of a Notice of Allowance are earnestly solicited.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. 1.16 or 1.17 to Deposit Account No. 50-2504. The Examiner is invited to contact the undersigned at 434-972-9988 to discuss any matter regarding this application.

Respectfully submitted,

Michael Haynes PLC



Date: 26 August 2005

Michael N. Haynes
Registration No. 40,014

1341 Huntersfield Close
Keswick, VA 22947
Telephone: 434-972-9988
Facsimile: 815-550-8850